What is claimed is:

1. An information processing apparatus comprising:

a first processor;

a second processor;

an application program, under control of the first processor, issuing a processing execution request to the second processor;

an actual processing section, under control of the second processor, executing an application interface processing code defined by the second processor; and

an interface that, when an execution request of the application interface processing is issued by the application program, sends the processing execution request to the actual processing section through a communication bus.

2. The information processing apparatus according to claim 1, wherein the second processor is a stream processor.

3. The information processing apparatus according to claim 1, wherein the first processor is a central processing unit (CPU).

4. The information processing apparatus according to claim 1, further comprising:

a driver, under control by the second processor, executing a device driver interface processing code defined by the second processor; and

an interface that, when an execution request of

the device driver interface processing code is issued by the application program, sends the execution request to the driver through the communication bus.

5. An information processing apparatus comprising:

a CPU;

a communication bus;

a bridge device coupled to the CPU and the communication bus, the bridge device includes a graphics controller to transmit graphic data;

a stream processor coupled to the communication bus, the stream processor processing stream data;

a video bus coupled to both the graphics controller and the stream processor; and

means for transferring (i) graphics data from the graphics controller to the stream processor through the video bus and (ii) transparent display information designating a rectangular region in a drawing area and a transparency rate at transparent display of the graphic data on a screen from the graphics controller to the stream processor through the communication bus, under control of the CPU.

6. The information processing apparatus according to claim 5, wherein the stream processor superposes the graphic data transferred through the video bus on a video image, in accordance with the rectangular region and the transparency rate represented by the

transparent display information transferred through the communication bus.

7. The information processing apparatus according to claim 5, wherein the communication bus is a Peripheral Component Internet (PCI) bus.

8. An information processing apparatus comprising:

a first processor;

a communication bus;

a bridge device coupled between the first processor and the communication bus;

a second processor coupled to the communication bus, the second processor processing stream data; and

control logic coupled to the communication bus and which, when a power-on signal is detected, issues a reset signal to each of the second processor and the first processor through the communication bus and issues a reset release signal to the first processor after issuing a reset release signal to the second processor.

9. The information processing apparatus according to claim 8, wherein the control logic is a system control microcomputer.

10. The information processing apparatus according to claim 8, wherein the first processor is a central processing unit, the second processor is a stream processor and the communication bus is a Peripheral

Component Interconnect (PCI) bus.

11. The information processing apparatus according to claim 8, wherein the control logic monitors the communication bus and determines whether or not the second processor is normally started by confirming whether or not an access to the communication bus is issued by the second processor.

12. The information processing apparatus according to claim 11, wherein the control logic monitors the communication bus, and resets and restarts the second processor and the first processor if there is no access from any one of the second processor and the first processor to the communication bus after a certain time has passed.

13. An information processing apparatus comprising:

a first processor;

a communication bus;

a bridge device coupled between the first processor and the communication bus, the bridge device including a first Media Independent Interface/Media Dependant Interface (MII/MDI) processing section; and

a second processor including a second MII/MDI processing section to communicate with the first MII/MDI processing section in communications with a network.

14. The information processing apparatus according

to claim 13, wherein the first processor is a CPU and the second processor is a network processor.

15. An information processing apparatus comprising:

a communication bus;

an interface coupled to the communication bus, the interface including a first Media Independent Interface/Media Dependant Interface (MII/MDI) processing section; and

a second processor including a second MII/MDI processing section adapted for communications with the first MII/MDI processing section and a network.

16. An information processing apparatus comprising:

a CPU;

a communication bus;

a first bridge device coupled between the CPU and the communication bus;

a stream processor coupled to the communication bus, the stream processor processing stream data;

a flash memory; and

a second bridge device coupled to the communication bus and the flash memory.

17. The information processing apparatus according to claim 16, wherein the CPU is adapted to access the flash memory through the first bridge device and the second bridge device.